TPS56637 4.5-V to 28-V Input, 6-A Synchronous Buck Converter

1 Features

- 4.5-V to 28-V Wide Input Voltage Range
- 0.6-V to 16-V Wide Output Voltage Range
- 6-A Maximum Continuous Output Current
- 500-kHz Switching Frequency
- Integrated 26-mΩ and 12-mΩ MOSFETs
- Supports POSCAP and All MLCC Output Capacitors
- D-CAP3™ Control Mode for Fast Transient Response
- Selectable Forced Continuous Conduction Mode (FCCM) for Tight Output Ripple or Auto-Skipping Eco-mode™ for Light-Load Efficiency
- 0.6-V ±1% Reference Voltage
- Internal 2-ms Soft Start
- Built-In Output Discharge Function
- Power Good Indicator to Monitor Output Voltage
- Non-Latched Output OV, UV, OT Protection for Fault Protection
- –40°C to +150°C Operating Junction Temperature
- Small 10-Pin 3.0-mm × 3.0-mm HotRod™ QFN Package

2 Applications

- Personal Printers, Multi-function Printers
- DTVs
- Monitors
- Industrial Computers

3 Description

The TPS56637 is an adaptive on-time D-CAP3™ control mode synchronous step-down DC-DC converter that can deliver 6-A continuous output current. The Eco-mode™ control scheme (pulse-skipping) optimizes this switch-mode power supply (SMPS) device for applications that require very-low power consumption, such as printers, DTVs, and monitors. The TPS56637 has 30-V capable MOSFETs for applications working at 24-V bus power lines. The D-CAP3™ control mode provides an easy-to-design, stable regulation with very little external components. It supports cost effective ceramic capacitors.

The TPS56637 has both FCCM and the Eco-mode™ control scheme for selection at light-load operation so that it can be used in a wider range of applications. The D-CAP3™ control mode can support an output up to 16 V.

The TPS56637 features cycle-by-cycle current limit, non-latched protection under overvoltage, undervoltage and overtemperature conditions.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS56637	VQFN-HR (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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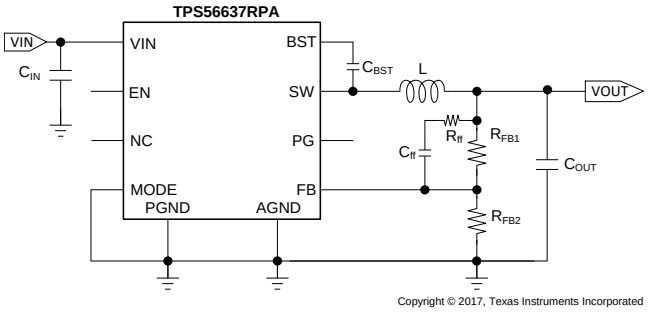
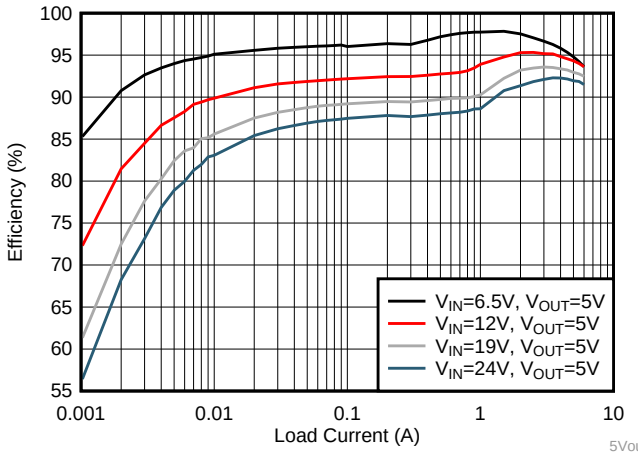
Simplified Schematic



TPS56637 Efficiency



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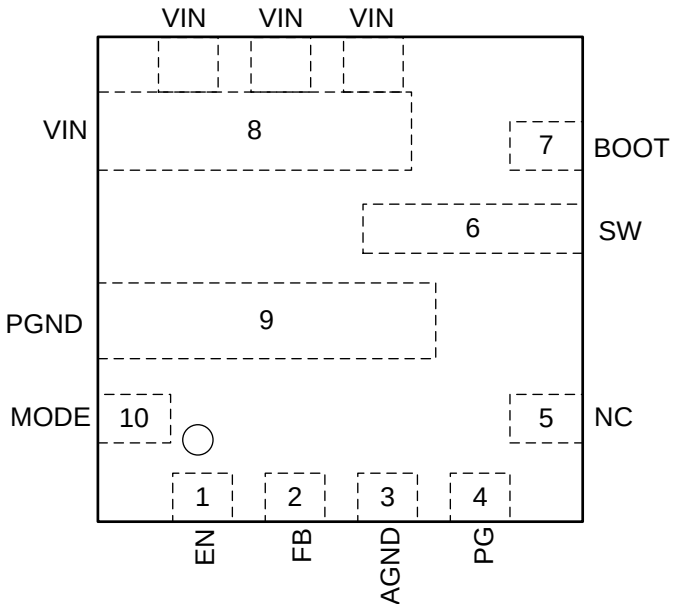
4 Revision History

DATE	REVISION	NOTES
July 2018	*	Advance Product release.

5 Pin Configuration and Functions

RPA Package
10-Pin VQFN-HR
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	EN	I	Enable input control, leaving this pin floating enables the converter. It also can be used to adjust the input UVLO by connecting to the resistor divider between VIN and EN. When choose resistor divider, need make sure V_{EN} voltage lower than its max recommended operation voltage 5.5V.
2	FB	I	Output feedback. Connect to the resistor divider between output voltage and GND.
3	AGND	G	Ground of internal analog circuitry. Connect AGND to PGND plane at a single point.
4	PG	O	Open Drain Power Good Indicator, it is asserted low if output voltage is out of PG threshold due to overvoltage, dropout, thermal shutdown, EN shutdown or during soft-start.
5	NC	N	Not Connected
6	SW	O	Switching node terminal. Connect the output inductor to this pin with wide and short tracks
7	BOOT	I	Supply input for the gate drive voltage of the high-side MOSFET. Connect a 0.1uF bootstrap capacitor between BOOT and SW.
8	VIN	P	Input voltage supply pin. Drain terminal of high side MOSFET. Connect the input decoupling capacitors between VIN and GND.
9	PGND	G	Power GND terminal. Source terminal of low side MOSFET.
10	MODE	I	Operation mode selection pin. Leaving this pin floating(>350kΩ) forces the TPS56637 into FCCM. Connecting this pin to GND(<50kΩ) forces the TPS56637 into Eco-mode™ under light load.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	V_{IN}	-0.3	30	V
	BOOT	-0.3	36	V
	BOOT (vs SW)	-0.3	6.0	V
	EN, FB, MODE	-0.3	6.0	V
	PGND, AGND	-0.3	0.3	V
Output voltage	SW	-0.3	30	V
	SW (10 ns transient)	-4	30	V
	PG	-0.3	6	V
Operating junction temperature, T_J		-40	150	°C
Storage temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input Voltage	V_{IN}	4.5		28	V
	BOOT	4.5		33.5	V
	BOOT (vs SW)	-0.1		5.5	V
	EN, FB, MODE	-0.1		5.5	V
	PGND, AGND	-0.1		0.1	V
Output Voltage	SW	-0.1		28	V
	PG	-0.1		5.5	V
Operating junction temperature, T_J		-40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS56637 QFN HOTROD 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

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6.5 Electrical Characteristics

T_J = –40°C to 150°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_Q	Operating – non-switching supply current	T_J=25°C, V_{EN}=5 V, V_{FB} = 0.7 V		125		µA
I_{OFF}	Shutdown supply current	T_J=25°C, V_{EN}=0 V		2		µA
UVLO						
UVLO	V_{IN} Under-Voltage Lockout	Wake up V_{IN} voltage	4.0	4.2	4.4	V
		Shut down V_{IN} voltage	3.4	3.6	3.8	V
		Hysteresis V_{IN} voltage		600		mV
ENABLE(EN PIN)						
I_{EN_INPUT}	Input current	V_{EN} = 1.1V		1		µA
I_{EN_HYS}	Hysteresis current	V_{EN} = 1.3V		4		µA
$V_{EN(ON)}$	Enable threshold	EN rising		1.23	1.29	V
$V_{EN(OFF)}$		EN failling	1.04	1.12		V
FEEDBACK VOLTAGE						
V_{FB}	Feedback voltage	V_{OUT} = 5V, continuous mode operation, T_J=25°C	0.594	0.6	0.606	V
		V_{OUT} = 5V, continuous mode operation, T_J=-40°C to 150°C	0.591	0.6	0.609	V
$I_{(VFB)}$	V_{FB} input current	V_{FB} = 0.7V, T_J = 25°C	-0.15	0	0.15	µA
MOSFET						
$R_{DS(on)h}$	High side switch resistance	T_J = 25°C, V_{BST} - V_{SW} = 5 V		26		mΩ
$R_{DS(on)l}$	Low side switch resistance	T_J = 25°C		12		mΩ
CURRENT LIMIT						
I_{OCL}	Valley current limit		6.3	7.5	8.6	A
I_{OC_REV}	Reverse current limit for FCCM Mode		2.3	3	3.7	A
POWER GOOD						
V_{PGTH}	PG Threshold	V_{FB} falling (Fault)		85%		
		V_{FB} rising (Good)		90%		
		V_{FB} falling (Good)		110%		
		V_{FB} rising (Fault)		115%		
I_{PGSINK}	PG sink current	V_{FB} = 0.5V, V_{PG} = 0.5V		1.5		mA
I_{PGLK}	PG leakage current	V_{PG} = 5.5V, V_{OUT} = 5.1V	-1		1	µA
FREQUENCY						
F_{SW}	Switching frequency	V_{IN}=12V, V_{OUT} =3.3V		500		kHz
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP threshold	OVP detect(L>H)		125%		
		Hysteresis		5%		
V_{UVP}	Output UVP threshold	Hiccup detect(H>L)		65%		
		Hysteresis		5%		
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Temperature Rising		165		°C
		Hysteresis		30		°C
SW DISCHARGE RESISTANCE						
R_{DISCHG}	V_{OUT} discharge resistance	V_{EN}=0, V_{SW}=0.5V, T_J=25°C		200		Ω

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6.6 Timing Requirements

T_J = –40°C to 150°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ON-TIME TIMER CONTROL						
$t_{ON(MIN)}$	Minimum on time(1)			50		ns
$t_{OFF(MIN)}$	Minimum off time	V_{FB} = 0.5 V, measure SW at 50% V_{IN}, Eco-mode		180	300	ns
SOFT START						
T_{SS}	Soft start time	Internal soft-start time		2		ms
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
T_{ON}	UV protection wait Time	UV triggered (V_{FB} lower than 65% V_{FB_nom})		0.25		ms
T_{OFF_OC}	UV protection recover time			25		ms

(1) Not production tested

6.7 Typical Characteristics

V_{IN} = 12 V (unless otherwise noted)

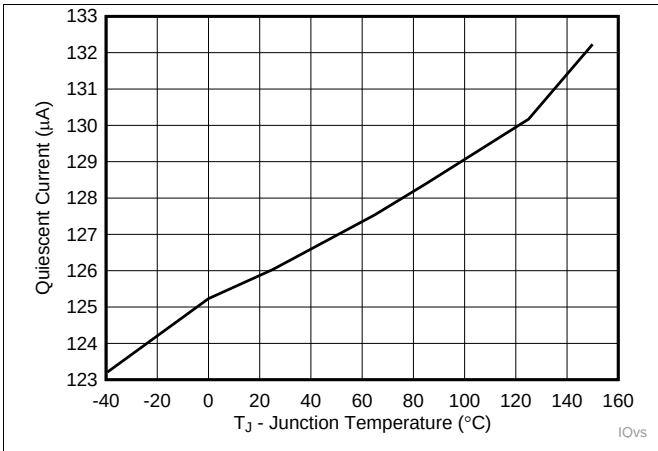

Figure 1. Quiescent Current vs Temperature

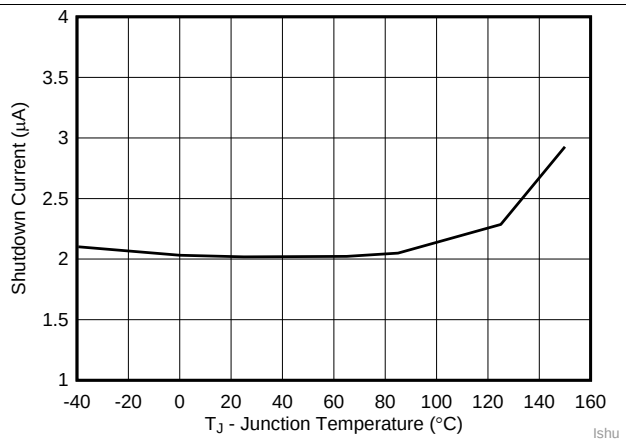

Figure 2. Shutdown Current vs Temperature

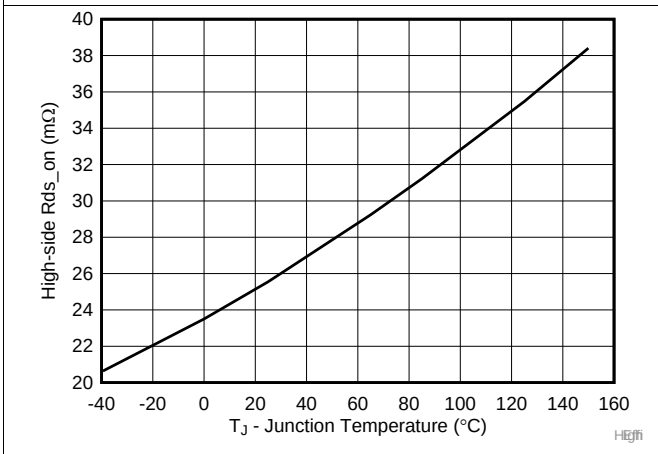

Figure 3. High-Side $R_{DS(on)}$ vs Temperature

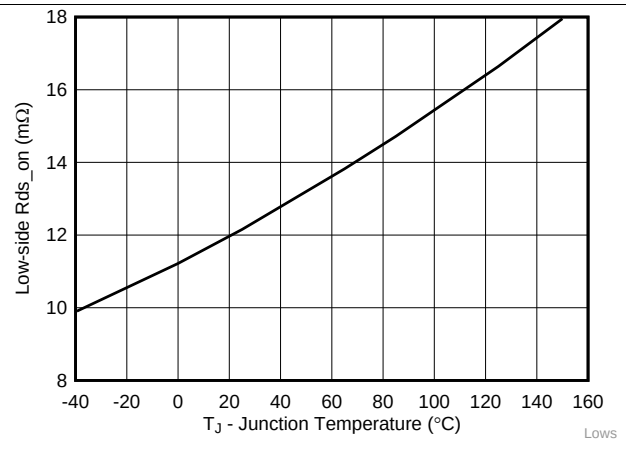

Figure 4. Low-side $R_{DS(on)}$ vs Temperature

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Typical Characteristics (continued)

V_{IN} = 12 V (unless otherwise noted)

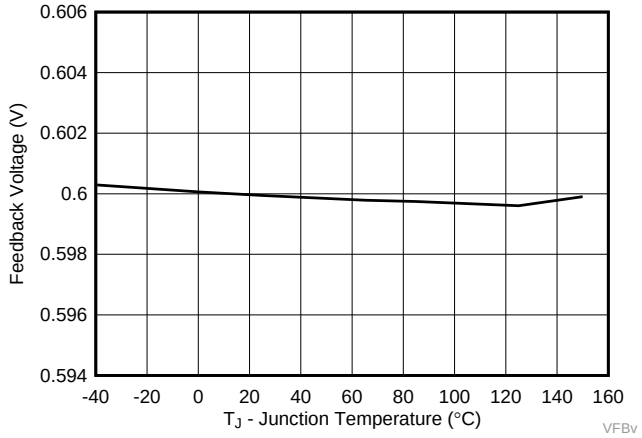

Figure 5. Feedback Voltage vs Temperature

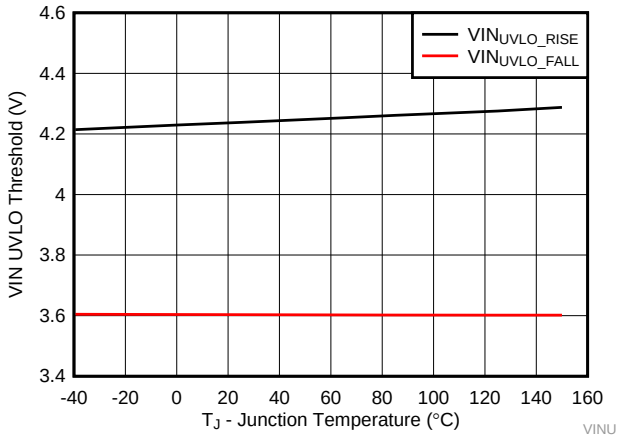

Figure 6. VIN UVLO Threshold vs Temperature

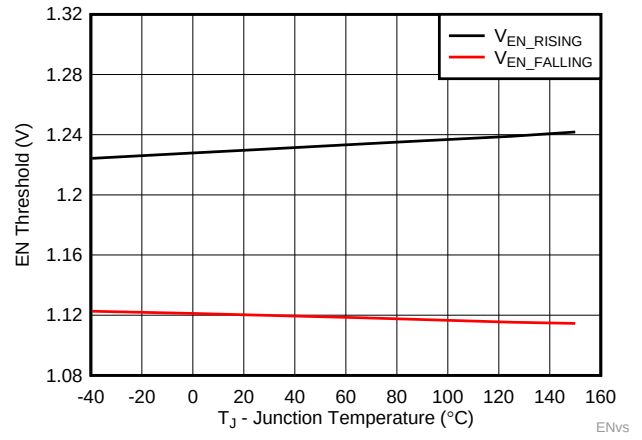

Figure 7. EN Threshold vs Temperature

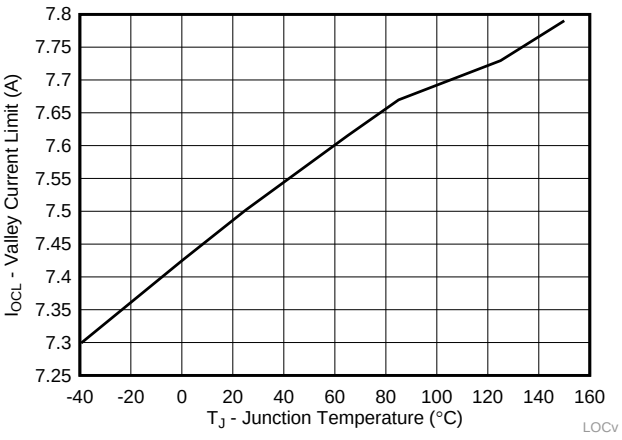

Figure 8. Valley Current Limit vs Temperature

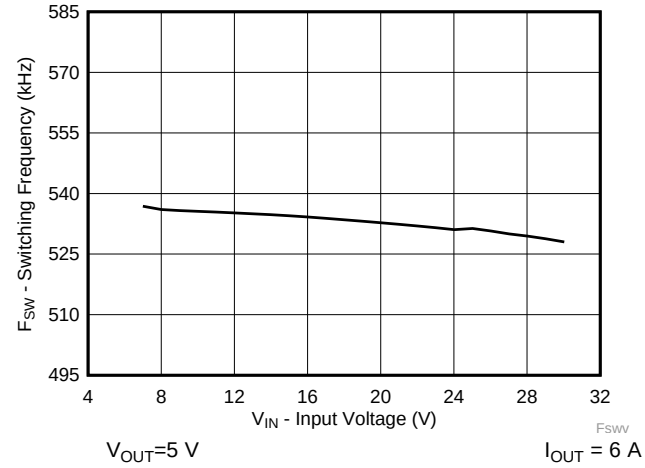

Figure 9. D-CAP3™ Switching Frequency vs Input voltage

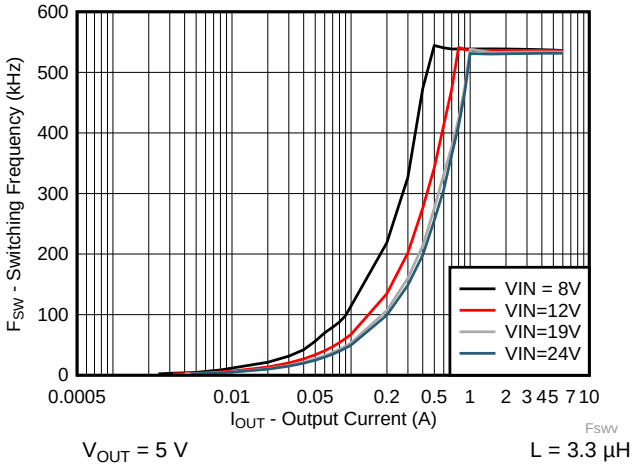

Figure 10. D-CAP3™ Switching Frequency vs Output Current

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Typical Characteristics (continued)

V_{IN} = 12 V (unless otherwise noted)

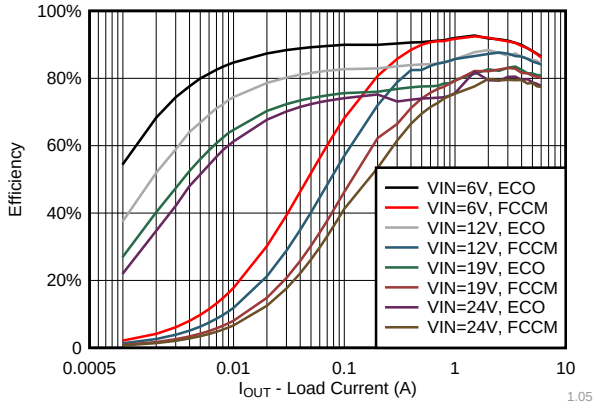

Figure 11. VOUT=1.05V Efficiency, L=1uH

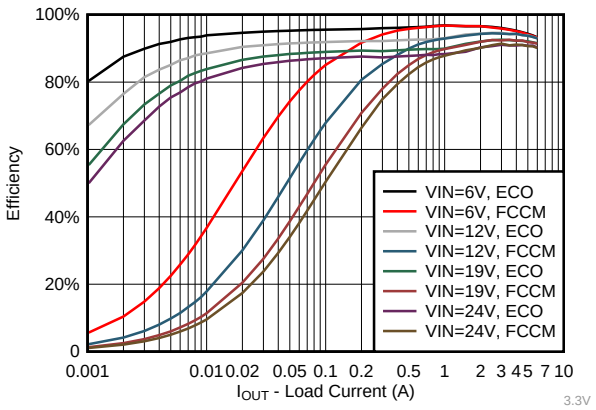

Figure 12. VOUT=3.3V Efficiency, L=2.2uH

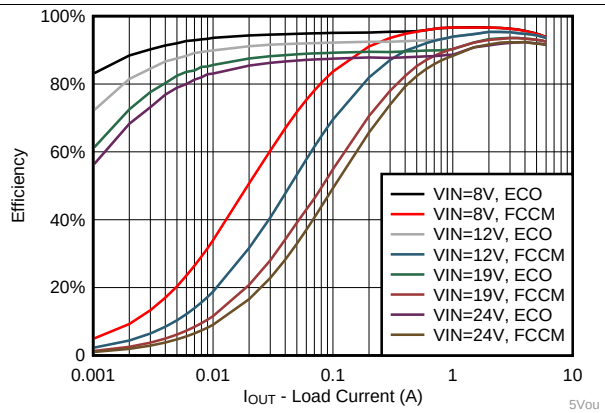

Figure 13. VOUT=5V Efficiency, L=3.3uH

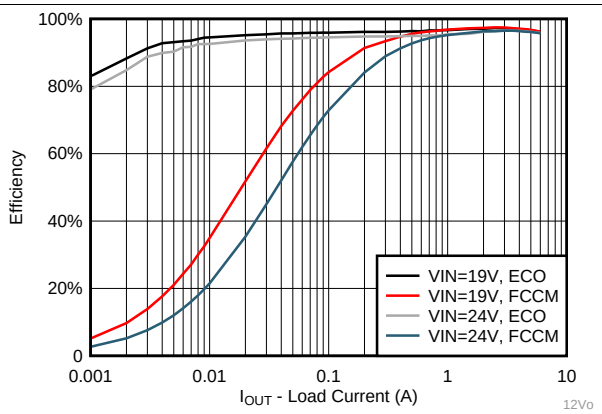

Figure 14. VOUT=12V Efficiency, L=4.7uH

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7 Detailed Description

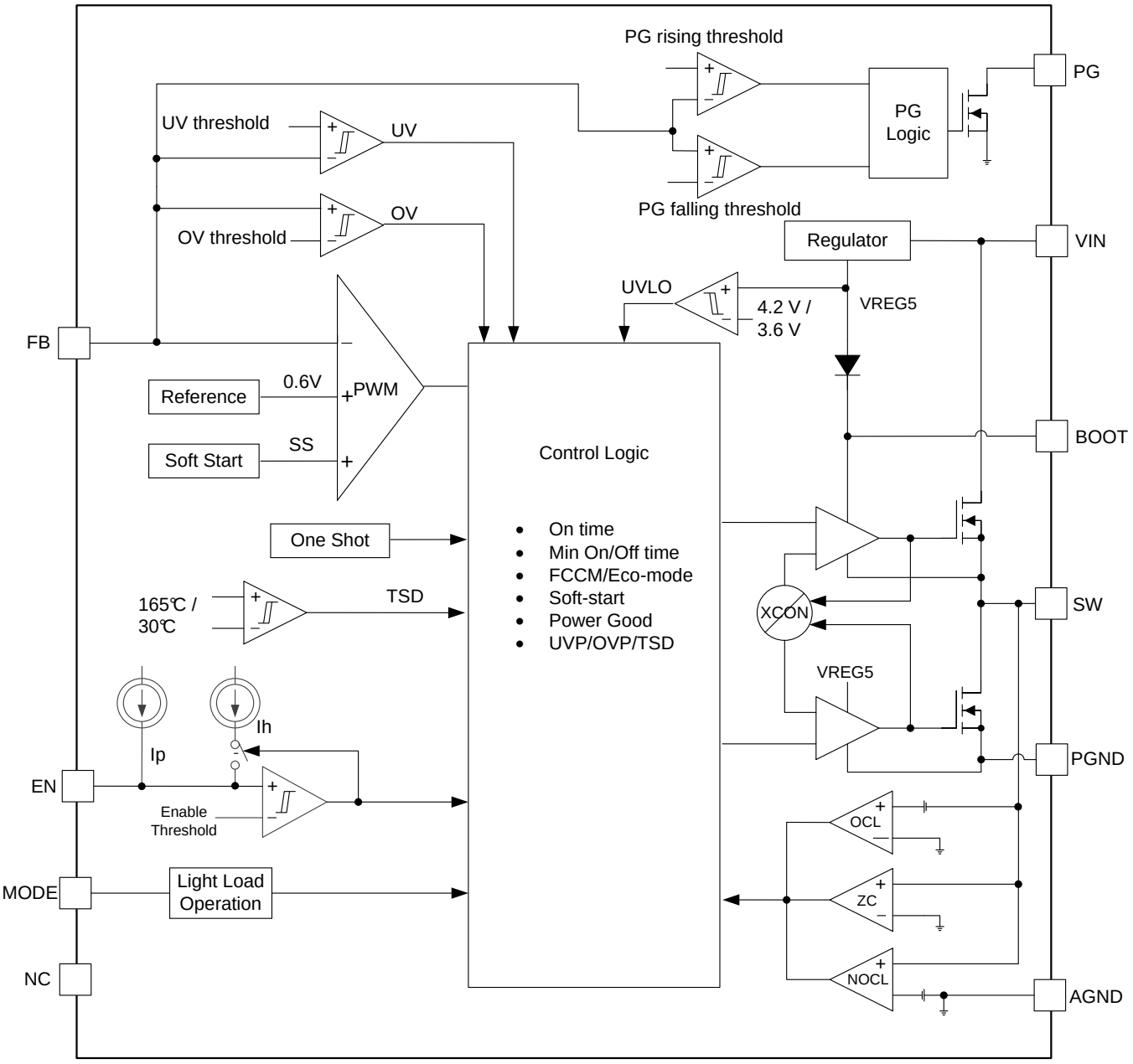
7.1 Overview

The TPS56637 is a high efficiency 6-A synchronous step-down converter. The proprietary D-CAP3™ control mode supports low ESR ceramic output capacitors without external compensation circuits. The fast transient response of D-CAP3™ Control Mode can reduce the output capacitance required to meet a specific level of performance.

In addition, MODE pin provides selectable forced continuous conduction mode (FCCM) for tight output ripple or auto-skipping Eco-mode™ for light load efficiency.

The device output can support up to 16V due to two stage ripple injection implement. The device is protected from over voltage, under voltage and over temperature conditions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 The Adaptive On-Time Control and PWM Operation

The main control loop of the TPS56637 is an adaptive on-time pulse width modulation controller that supports a proprietary D-CAP3™ control mode. The D-CAP3™ control mode combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

Feature Description (continued)

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one shot duration is set proportional to the converter input voltage, V_{IN}, and inversely proportional to the output voltage, V_O, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP3™ control mode.

7.3.2 Mode Selection

TPS56637 has a MODE pin that can offer 2 different states of operations under light load. If MODE pin is short to GND, TPS56637 works under Eco-mode™ control scheme. If MODE pin is floating, TPS56637 works under FCCM mode. The MODE pin will be detected and latched after EN pin toggles high, and then the internal soft-start function begins to ramp up the reference voltage to the PWM comparator. Once soft start is completed, the MODE pin will not change until VIN or EN toggles.

Table 1. MODE Pin Settings

MODE Pin	Light Load Operation Mode
Short to GND (<50kΩ)	Eco-mode™ control scheme
Floating (>350kΩ)	FCCM

7.3.2.1 Eco-mode™ Control Scheme

When MODE pin is short to GND, the TPS56637 is designed with Eco-mode™ control scheme to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in Equation 1

$$I_{OUT(LL)} = \frac{1}{2 \cdot L \cdot f_{SW}} \cdot \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN}} \quad (1)$$

7.3.2.2 FCCM Control

When MODE pin is floating, the TPS56637 is designed to operate in forced continuous conduction mode (FCCM) during light load conditions. During FCCM, the switching frequency is maintained at an a quasi-fixed level over the entire load range which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load. For some audio application, this mode can help avoid switching frequency drop into audible range that may introduce some "noise".

7.3.3 Soft Start and Pre-Biased Soft Start

The TPS56637 has an internal 2ms soft-start. When the EN pin becomes high and the MODE pin's reading and setting are finished , the internal soft-start function begins ramping up the reference voltage to the PWM comparator. If the output capacitor is pre-biased at startup, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converters ramp up smoothly into regulation point.

7.3.4 Enable and Adjusting Undervoltage Lockout

The EN pin provides electrical on and off control of the device. When the EN pin voltage exceeds the threshold voltage, the device begins operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters the low-quiescent (I_Q) state.

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The EN pin has an internal pull-up current source which allows the user to float the EN pin to enable the device. If an application requires control of the EN pin, use open-drain or open-collector output logic to interface with the pin.

The device implements internal undervoltage-lockout (UVLO) circuitry on the V_{IN} pin. The device is disabled when the VIN pin voltage falls below the internal V_{IN} UVLO threshold. The internal V_{IN} UVLO threshold has a hysteresis of 600 mV.

If an application requires a higher UVLO threshold on the VIN pin, then the EN pin can be configured as shown in Figure 15. When using the external UVLO function, setting the hysteresis at a value greater than 600 mV is recommended.

The EN pin has a small pull-up current, I_p, which sets the default state of the pin to enable when no external components are connected. The pull-up current is also used to control the voltage hysteresis for the UVLO function because it increases by I_h when the EN pin crosses the enable threshold. Use Equation 2 , and Equation 3 to calculate the values of R1 and R2 for a specified UVLO threshold. Once R1, R2 settled down, the V_{EN} voltage need to be calculated by Equation 4 to make sure that it is lower than 5.5V with max V_{IN}, max I_p and max I_h.

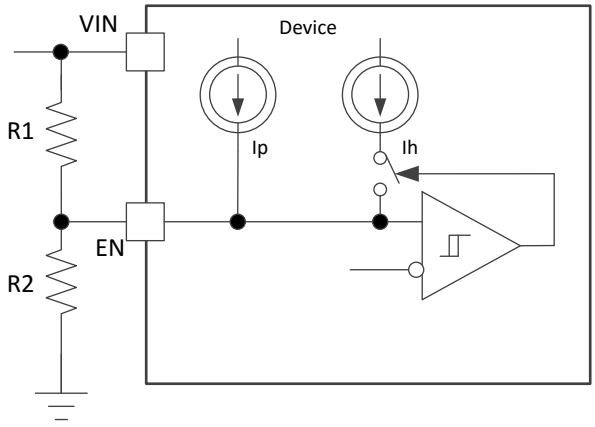

Figure 15. Adjustable VIN Undervoltage Lockout

$$R_1 = \frac{V_{START}\frac{V_{ENfalling}}{V_{ENrisig}} - V_{STOP}}{I_p\left(1 - \frac{V_{ENfalling}}{V_{ENrising}}\right) + I_h} \quad (2)$$

$$R_2 = \frac{R_1 \times V_{ENfalling}}{V_{STOP} - V_{ENfalling} + R_1\left(I_p + I_h\right)} \quad (3)$$

$$V_{EN} = \frac{R_2 \times V_{IN} + R_1 R_2\left(I_p + I_h\right)}{R_1 + R_2} \quad (4)$$

Where

- I_p = 1 µA
- I_h = 4 µA
- $V_{ENfalling}$ = 1.17 V
- $V_{ENrising}$ = 1.21 V

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7.3.5 Current Protection and UV Protection

The output overcurrent limit (OCL) is implemented using a cycle by cycle valley detect control circuit. The switch current is monitored during off state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switching current. During the on time of the high-side FET switch, the switch current increases at a linear rate determined by input voltage, output voltage, the on-time and the output inductor value. During the on time of the low side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the measured drain to source voltage of low-side FET is above the voltage proportional to current limit, the low side FET stays on until the current level which reduces the output current available. When the current is limited the output voltage tends to drop because the load demands is higher than what converter can support. When the output voltage falls below 65% of the target voltage, the UVP comparator detects it and shuts down the device after a wait time of 0.25ms, the device re-starts after a hiccup time of 25ms. In this type of valley detect control the load current is higher than the OCL threshold by half of the peak to peak inductor current. When the over current condition is removed, the output voltage returns to the regulated value.

7.3.6 Overvoltage Protection

When output voltage exceeds the over-voltage protection threshold, both high side and low side FET turn off, and the SW discharge path turns on. The device will not re-start until OVP event is removed (down by approximately "5%" hysteresis). After waiting for 25ms deglitch time, then re-soft-start process to power on the device will start.

7.3.7 UVLO Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut down. This protection is non-latching.

7.3.8 Thermal Shutdown

The device monitors the internal die temperature. If this temperature exceeds the thermal shutdown threshold value (typically 165°C) the device shuts off. This is a non-latch protection. During start up, if the device temperature is higher than 165°C the device does not start switching and does not load the mode settings. If the device temperature goes higher than TRIP threshold after start up, it shuts down device immediately. Hysteresis is built, the device turns on after the device has been cooled by approximately 30°C.

7.3.9 Power Good

The power good (PG) pin is an open drain output. Once the FB pin voltage is between 90% and 110% of the internal reference voltage (V_{REF}) the PG is de-asserted and floats after a 0.2ms deglitch time. A pullup resistor of 100kΩ is recommended to pull it up to like 5V voltage. The PG pin is pulled low when FB pin voltage is lower than V_{UVP} or greater than V_{OVP} threshold, or in an event of thermal shutdown. The PG error (from high to low) deglitch time is 64µs.

7.4 Device Functional Modes

7.4.1 Standby Operation

The TPS56637 can be placed in standby mode by pulling the EN pin low. The device operates with a shutdown current of 2µA(typical) when in standby condition.

7.4.2 Normal Operation

When the input voltage is above the UVLO threshold voltage and EN pin is high, TPS56637 can operate in its normal switching modes. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0 A. In CCM, the TPS56637 operates at a quasi-fixed frequency of 500kHz (typical).

ADVANCE INFORMATION

Device Functional Modes (continued)

7.4.3 Light Load Operation

When the MODE pin is selected to operate in FCCM mode, the converter operates in continuous conduction mode (FCCM) during light-load conditions. During FCCM, the switching frequency is maintained at an almost constant level over the entire load range which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load. If the MODE pin is selected to operate in Eco-mode™ control scheme, the device enters pulse skip mode after the valley of the inductor ripple current crosses zero. The Eco-mode™ control scheme maintains higher efficiency at light load with a lower switching frequency. If the TPS56637 works at Eco-mode™ and the load current is light enough to a specific value, the TPS56637 will enter ULQ™ mode that the TPS56637 will disable some internal circuits to increase the light load efficiency more higher.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The schematic of Figure 16 shows a typical application for TPS56637. This design converts an input voltage range of 4.5 V to 28 V down to 5 V with a maximum output current of 6 A.

8.2 Typical Application

The application schematic in Figure 16 shows the TPS56637 4.5-V to 28-V Input, 5-V output converter design meeting the requirements for 6-A output. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

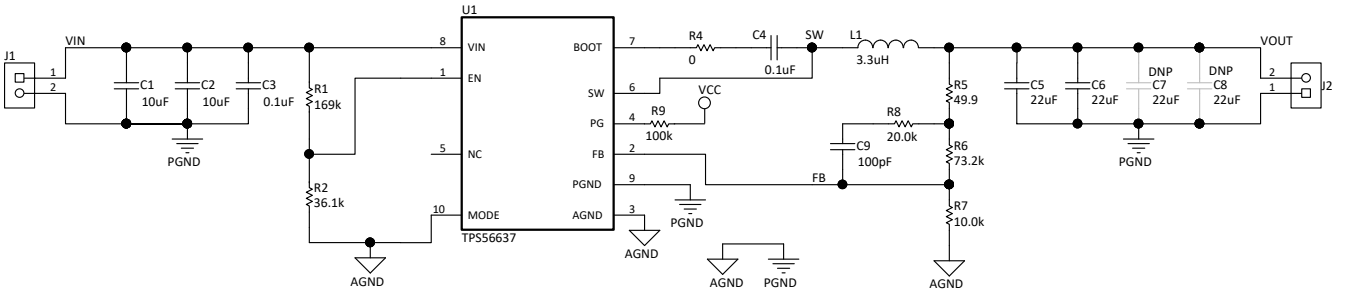


Figure 16. TPS56637 5-V, 6-A Reference Design

8.2.1 Design Requirements

Table 2 shows the design parameters for this application.

Table 2. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	4.5 to 28V
Output voltage	5V
Transient response, 6-A load step	ΔV_{OUT} = ±5%
Input ripple voltage	200 mV
Output ripple voltage	<30 mV
Output current rating	6A
Operating frequency	500 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the V_{FB} pin. TI recommends to use 1% tolerance or better divider resistors. Start by using Equation 5 to calculate V_{OUT}.

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the V_{FB} input current will be more noticeable.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R6}{R7}\right) \quad (5)$$

ADVANCE INFORMATION

8.2.2.2 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (6)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP3 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of Equation 6 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 3.

Table 3. Recommended Component Values

OUTPUT VOLTAGE (V)	R6 (kΩ)	R7 (kΩ)	L1 (µH)			C5 + C6 (µF)	C9 (pF)	R8 (kΩ)
			MIN	TYP	MAX			
1.05	7.5	10.0	TBD	1	TBD	66	TBD	TBD
1.2	10	10.0	TBD	1	TBD	66	TBD	TBD
1.8	20	10.0	TBD	1.2	TBD	66	TBD	TBD
3.3	45.3	10.0	TBD	2.2	TBD	44	100	20
5	73.2	10.0	TBD	3.3	TBD	44	100	20
12	191	10.0	TBD	4.7	TBD	66	68	20

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 7, Equation 8, and Equation 9. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

Use 500 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of Equation 8 and the RMS current of Equation 9.

$$Il_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \cdot \frac{V_{IN(MAX)} - V_{OUT}}{L_O \cdot f_{SW}} \quad (7)$$

$$Il_{PEAK} = I_O + \frac{Il_{P-P}}{2} \quad (8)$$

$$I_{LO(RMS)} = \sqrt{I_O^{\,2} + \frac{1}{12} Il_{P-P}^{\,2}} \quad (9)$$

For this design example, the calculated peak current is 6.86A and the calculated RMS current is 6.02 A. The inductor used is IHLP3232DZER3R3M11 with a peak current rating of 10.5A and an RMS current rating of 9.7A.

The capacitor value and ESR determines the amount of output voltage ripple. TheTPS56637 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 µF to 68 µF. Use Equation 10 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{\sqrt{12} \cdot V_{IN} \cdot L_O \cdot f_{SW}} \quad (10)$$

For this design two MuRata GRM32ER71E226KE15L 22-µF output capacitors are used. The calculated RMS current is 0.498A and each output capacitor is rated for 4 A.

8.2.2.3 Input Capacitor Selection

The TPS56637 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor (C3) from VIN to PGND pin is recommended to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage. The input voltage ripple can be calculated using Equation 11. Using the design example values, I_{outmax} = 6 A, C_{in} = 10 µF × 2, F_{sw}=500 kHz, yields an input voltage ripple of 150 mV.

$$\Delta V_{in} = \frac{I_{outmax} \cdot 0.25}{C_{in} \cdot f_{SW}} \tag{11}$$

8.2.2.4 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT to SW pin for proper operation. TI recommends to use a ceramic capacitor.

8.2.3 Application Curves

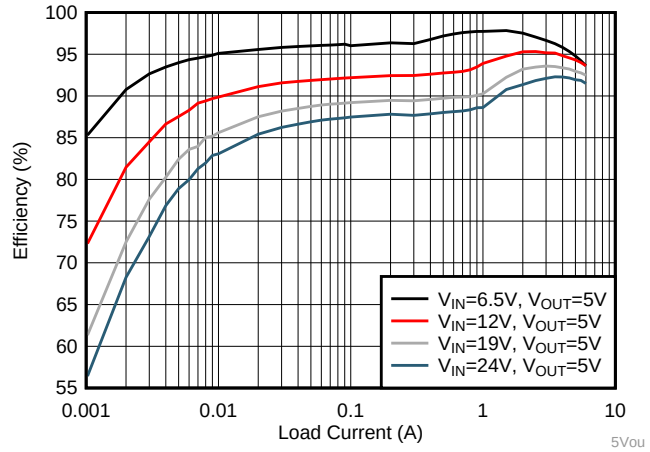


Figure 17. Efficiency

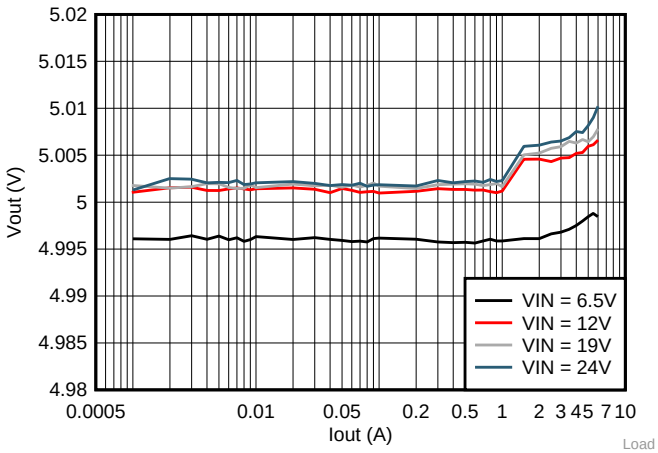


Figure 18. Load Regulation

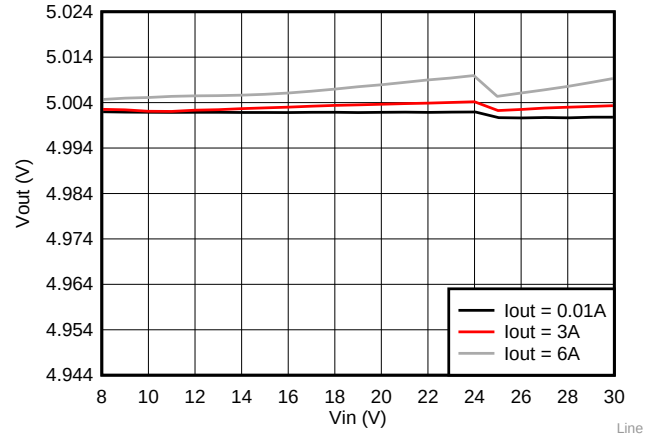


Figure 19. Line Regulation

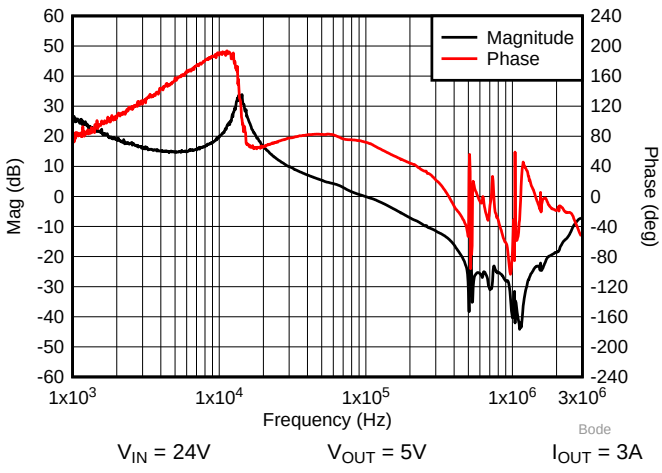


Figure 20. Bode Plot

ADVANCE INFORMATION

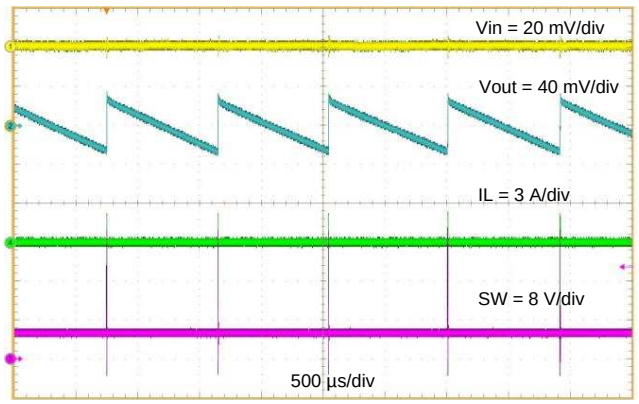


Figure 21. Steady State Waveforms, No Load

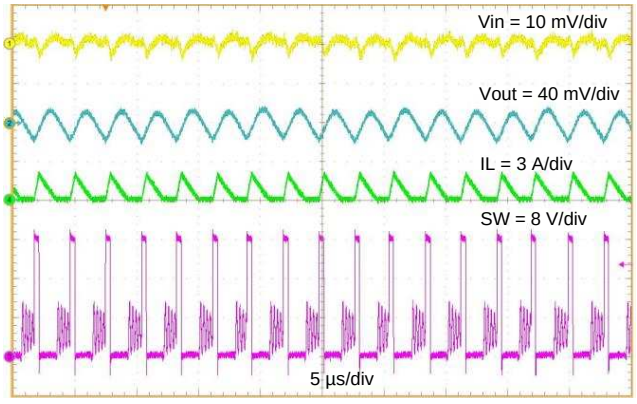


Figure 22. Steady State Waveforms, I_{OUT} 0.6 A

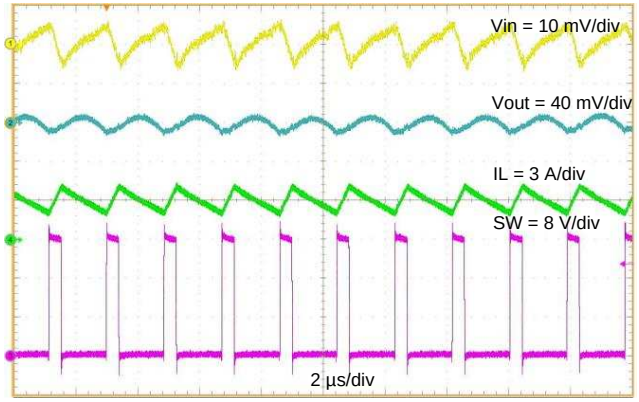


Figure 23. Steady State Waveforms, I_{OUT} 3 A

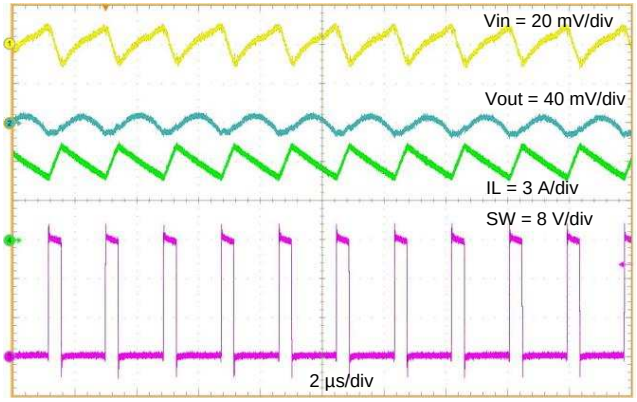


Figure 24. Steady State Waveforms, I_{OUT} 6 A

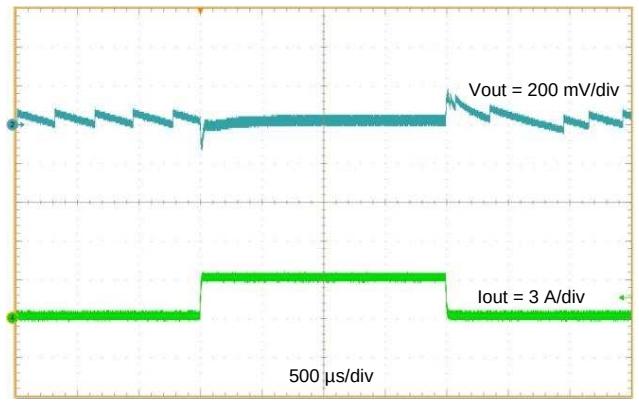


Figure 25. Transient Response 0 to 3 A

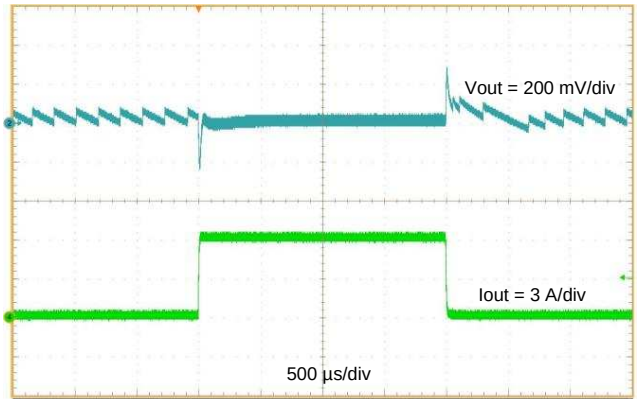


Figure 26. Transient Response 0 to 6 A

ADVANCE INFORMATION

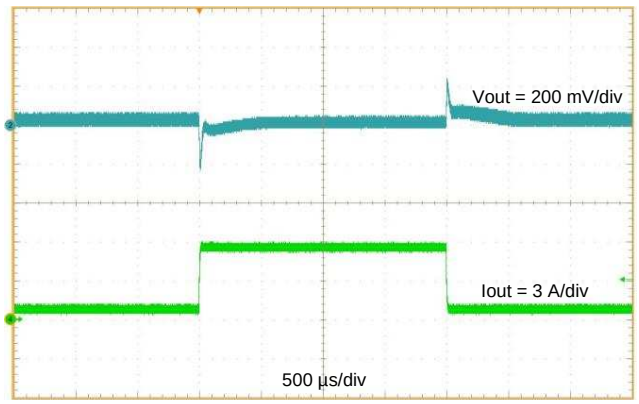


Figure 27. Transient Response 0.6 to 5.4 A

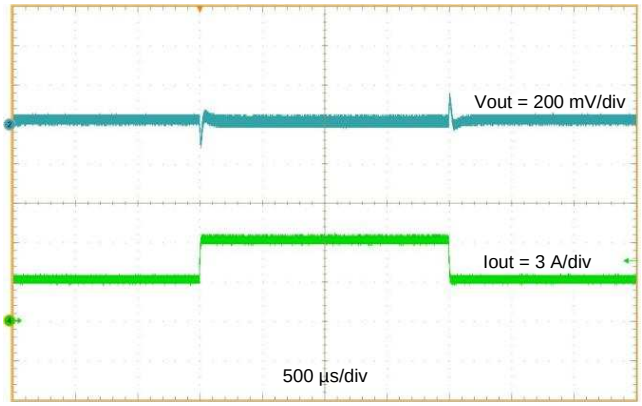


Figure 28. Transient Response 3 to 6 A

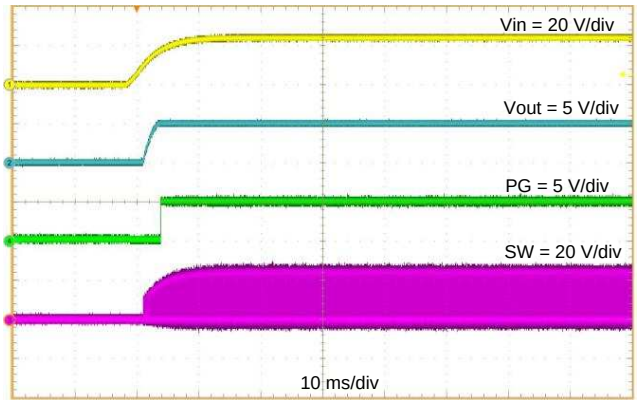


Figure 29. Startup Relative to V_{IN}

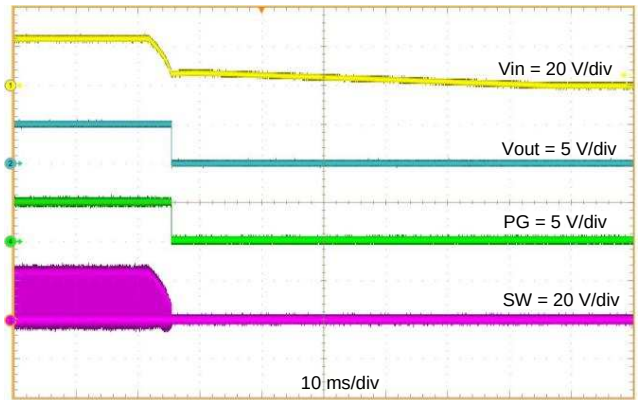


Figure 30. Shutdown Relative to V_{IN}

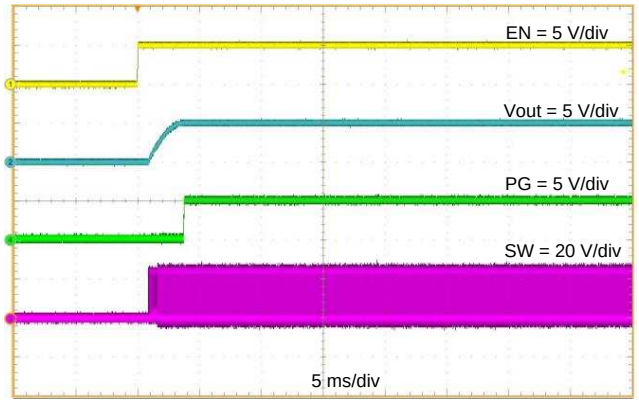


Figure 31. Enable Relative to EN

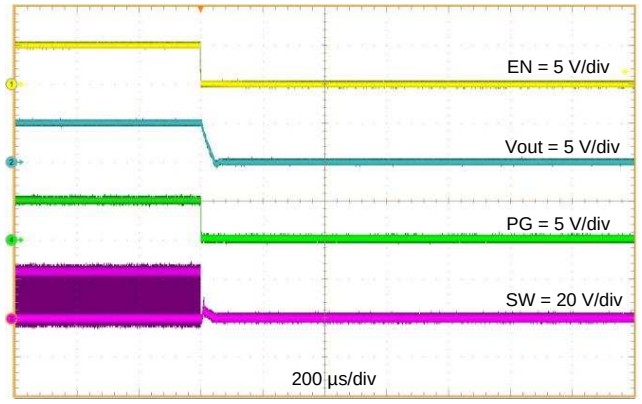


Figure 32. Disable Relative to EN

ADVANCE INFORMATION

9 Power Supply Recommendations

The TPS56637 is designed to operate from input supply voltage in the range of 4.5 V to 28 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far from the TPS56637 circuit, some additional input bulk capacitance is recommended.

10 Layout

10.1 Layout Guidelines

1. Recommend a four-layer or six-layer PCB for good thermal performance and with maximum ground plane. 3"x 3", four-layer PCB with 2-oz. copper used as example.
2. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
3. Putting at least two vias for VIN and GND traces, and as close as possible to the pins, which will make higher improvement of the thermal
4. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
5. Provide sufficient vias for the input capacitor and output capacitor.
6. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
7. Do not allow switching current to flow under the device.
8. A separate VOUT path should be connected to the upper feedback resistor.
9. Make a Kelvin connection to the GND pin for the feedback path.
10. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
11. The trace of the VFB node should be as small as possible to avoid noise coupling.
12. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example

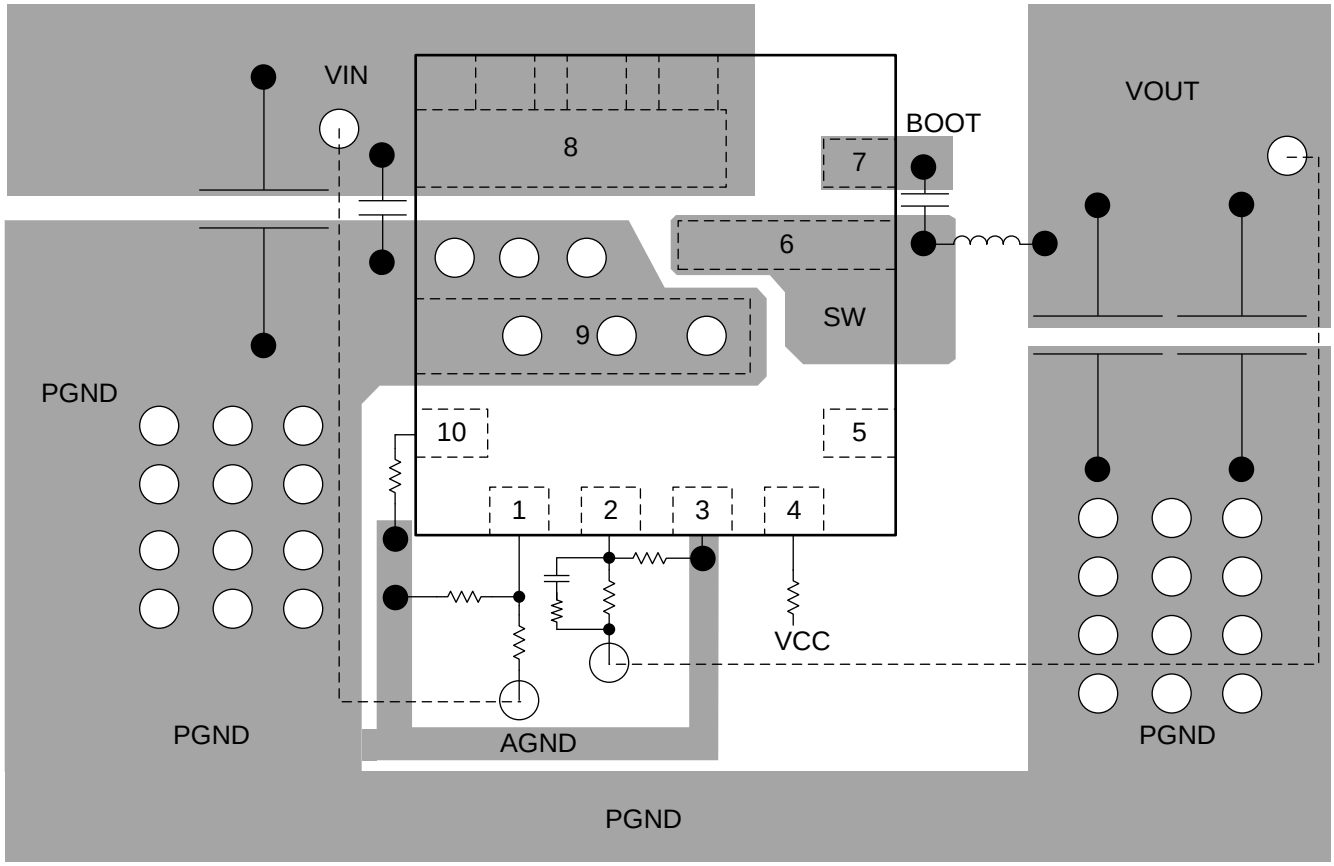


Figure 33. TPS56637 Layout

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following: Texas Instruments, *TPS56637EVM-029 6-A, Regulator Evaluation Module* user's guide

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

D-CAP3, Eco-mode, HotRod, ULQ, E2E are trademarks of Texas Instruments.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

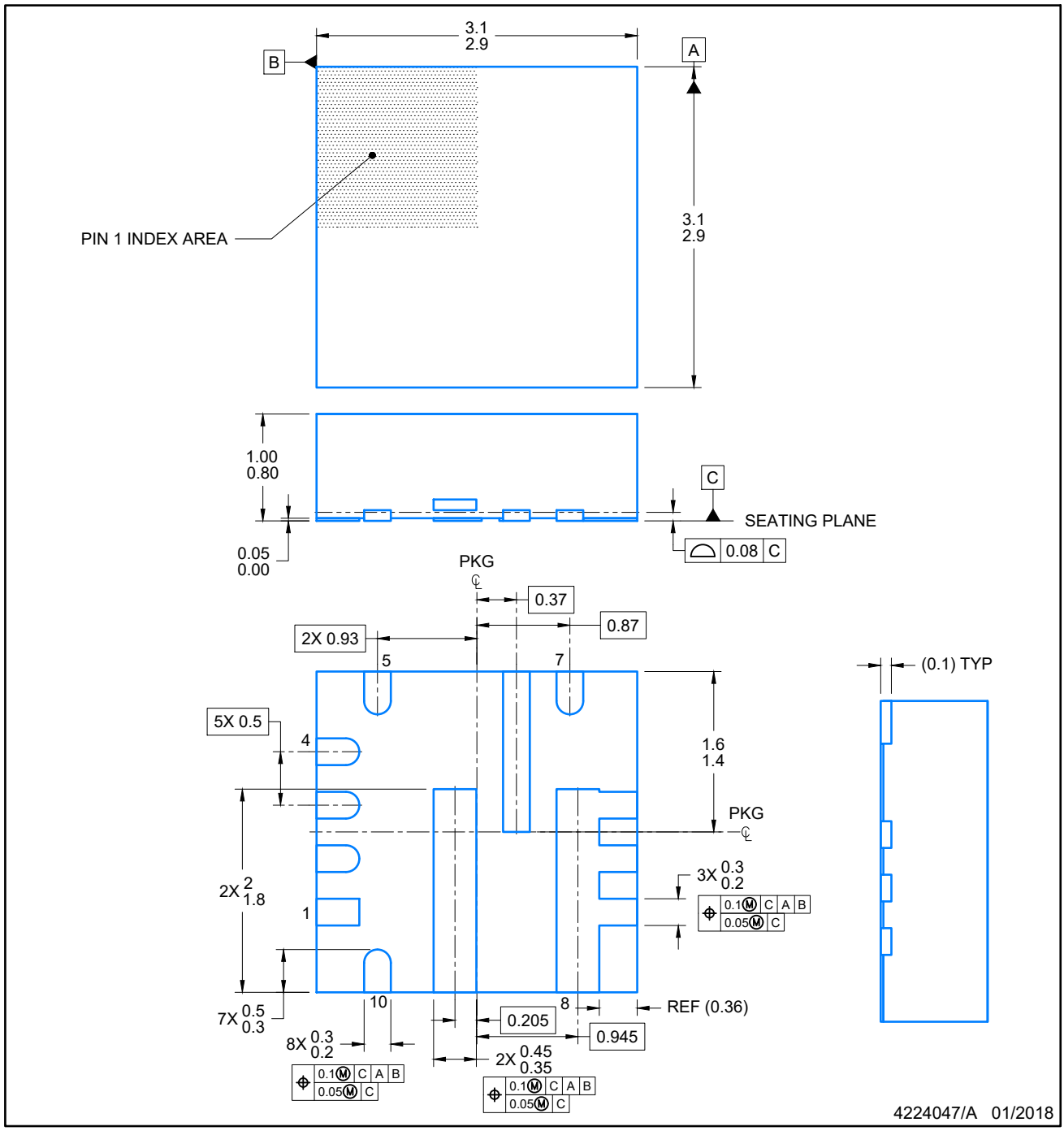
ADVANCE INFORMATION

PACKAGE OUTLINE

RPA0010A

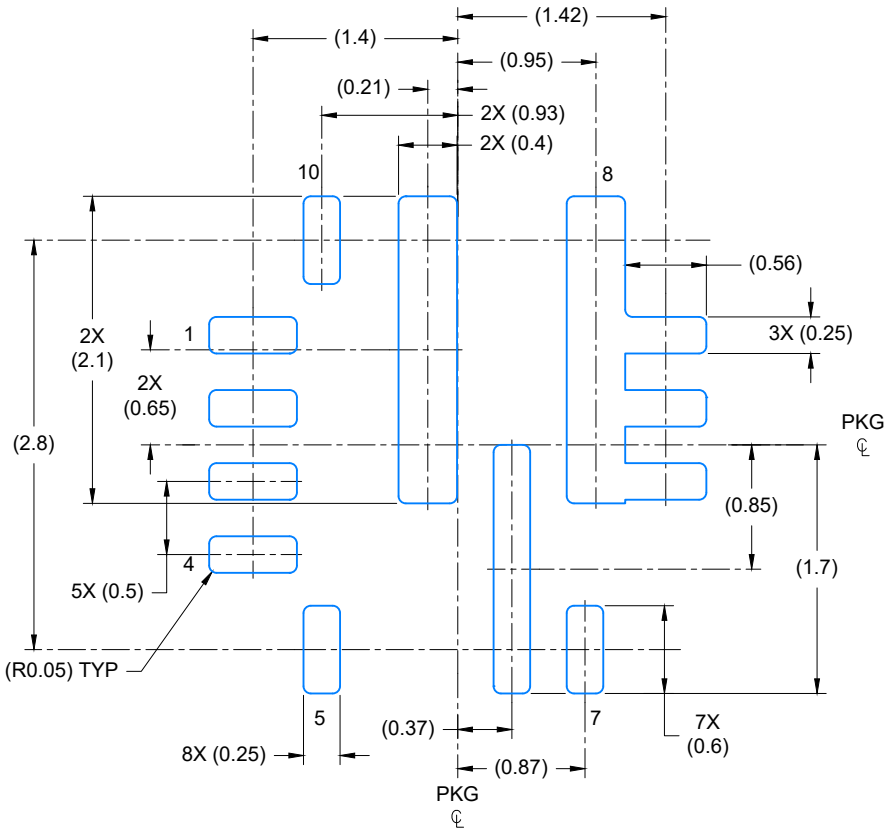
VQFN-HR - 1 mm max height

PLASTIC QUAD FLAT-NO LEAD

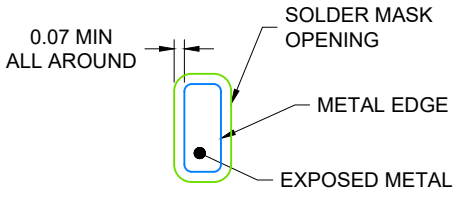


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

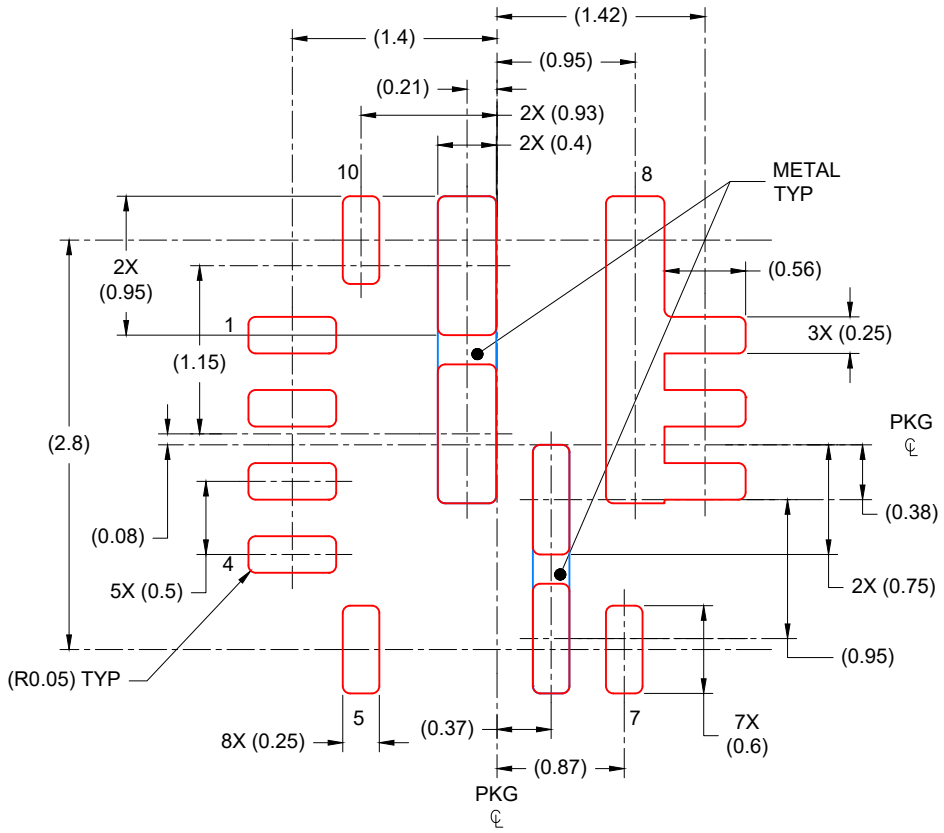


NON SOLDER MASK
DEFINED

4224047/A 01/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
PADS 6 and 9: 89% PRINTED COVERAGE BY AREA
SCALE: 20X

4224047/A 01/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking(5)(6)
XTPS56637RPAR	PRE_PROD	VQFN-HR	RPA	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	–40 to 125	X56637

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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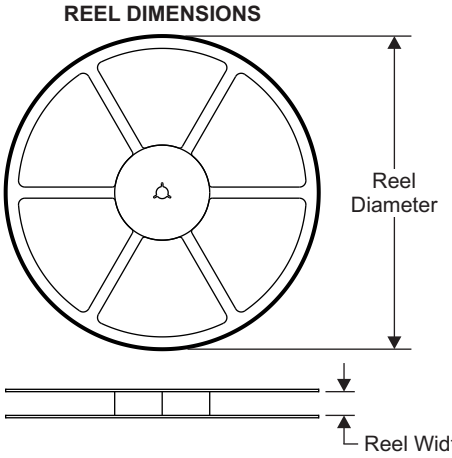
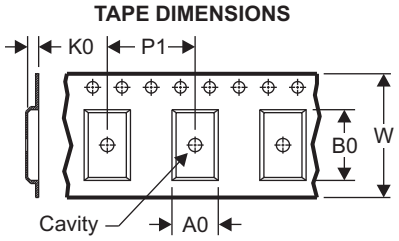
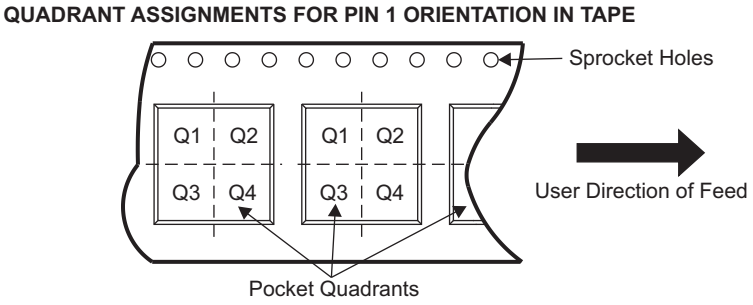
ADVANCE INFORMATION

12.1.2 Tape and Reel Information





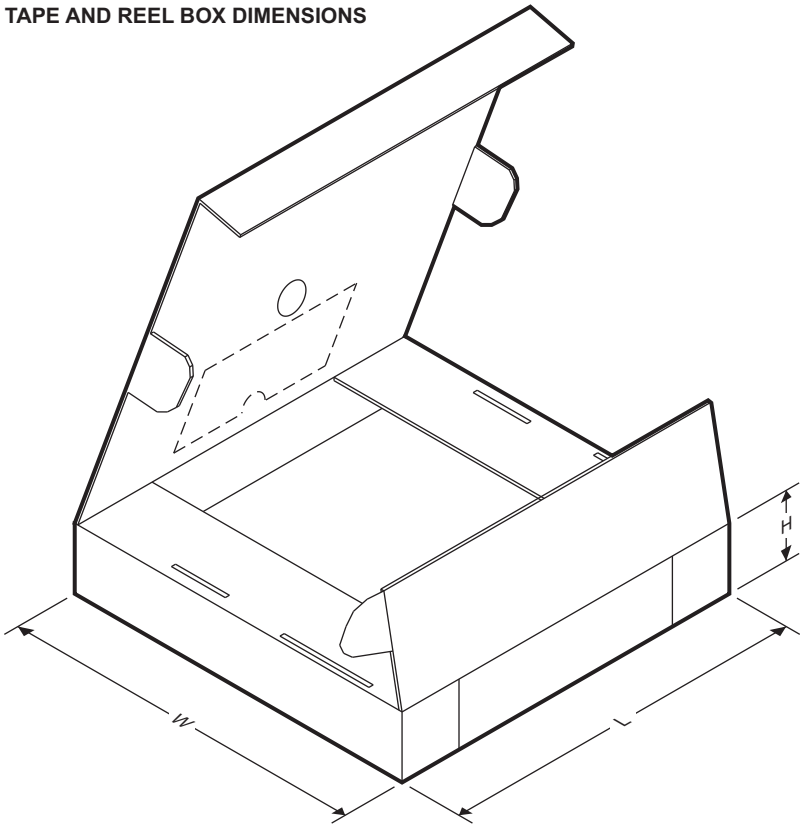
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTPS56637RPAR	VQFN-HR	RPA	10	3000	330	12	3.3	3.3	1.1	8	9.1	2

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTPS56637RPAR	VQFN-HR	RPA	10	3000	367	367	35

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS56637RPAR	PREVIEW	VQFN-HR	RPA	10	3000	TBD	Call TI	Call TI	-40 to 125		
XTPS56637RPAR	ACTIVE	VQFN-HR	RPA	10	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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